MIXER CIRCUIT WITH BYPASS AND MIXING MODES HAVING CONSTANT EVEN ORDER GENERATION AND METHOD OF OPERATION

Cross Reference to Related Applications

[0001] This application claims priority to, and hereby incorporates by reference in their entirety, the following patent applications:

[0002] U.S. Provisional Patent Application No. 60/433,066, filed on December 11, 2002, entitled INTEGRATED CROSSPOINT SWITCH WITH BAND TRANSLATION;

[0003] U.S. Provisional Patent Application No. 60/433,061, filed on December 11, 2002, entitled IN-LINE CASCADABLE DEVICE IN SIGNAL DISTRIBUTION SYSTEM WITH AGC FUNCTION;

[0004] U.S. Provisional Patent Application No. 60/433,067, filed on December 11, 2002, entitled NxM CROSSPOINT SWITCH WITH BAND TRANSLATION;

[0005] U.S. Provisional Patent Application No. 60/433,063, filed on December 11, 2002, entitled MIXER WITH PASS-THROUGH MODE WITH CONSTANT EVEN ORDER GENERATION.

Background

[0006] The present invention relates generally to mixer circuits, and in particular to a mixer circuit which can operate in either a bypass mode or mixing mode while retaining a high level of even order mixer product suppression.

[0007] Communication systems which transmit and receive signals often employ one or more mixing circuits to translate signals at a one frequency to another frequency. As known to the practitioner, the mixing circuits usually include two input ports for receiving two signals, typically identified as RF and LO signals, and an output port for providing a signal at the mixing product of the two input signals. As is well known, the mixing product of the two signals, typically referred to as the IF signal, may be expressed as:

$$IF = | Mf_{RF} \pm Nf_{LO}|$$

[0008] As can be seen, signals at multiple frequencies are produced during the mixing process, one of which is most often desired, e.g., a downconverted signal at frequency RF-LO. The presence of remaining signals at frequencies within the operational band of the mixer's output, conventionally referred to as "interferers," can be problematic, as they can interfere with the proper operation of the communication system. Accordingly, the elimination of unwanted interferers is an important design criterion in most systems.

[0009] Several mixer architectures are known in the art as providing rejection of at least some of the potentially interfering signals. For example, doubly balanced mixers are known in the art as providing excellent rejection of even order mixing products, a characteristic which makes the architecture ideal in a variety of communication systems.

[0010] Fig. 1A illustrates a simplified switch diagram of a doubly balanced mixer as known in the art. The mixer 100 includes RF and IF ports 110 and 130, respectively, each of which is shown differentially, but may be single-ended in another embodiment. The differential RF signal 110 is supplied to the input of SPDT switches 122, the states of which are switched at a rate determined by an LO signal 125 supplied thereto. The outputs of the switches 122 are coupled to differential IF ports 130 operable to provide the differential IF signal 130.

[0011] Fig. 1B illustrates the doubly balanced mixer of Fig. 1A as a Gilbert cell multiplier or mixer circuit known in the art. The mixer circuit includes two cross-coupled differential transistor pairs 122 whose base terminals are coupled to the LO source 125, collector terminals are coupled to the IF loads 130, and emitter terminals are coupled to buffer transistors 117. Responsive to the differential RF signal applied at terminals 110a and 110b, a voltage difference is established across resistor 115, resulting in the corresponding modulation of the quiescently-supplied current driving the transistor pairs 122 that comprise the mixer core. Those skilled in the art will appreciate that illustrated mixer circuit is only exemplary, and numerous variations of the circuit are also widely used.

[0012] While doubly balanced mixers provide a high level of even order mixing product suppression, circuit imperfections lead to degradation in that suppression. For example, a relatively low impedance parasitic 112 (e.g., capacitance) can load the emitter nodes of the mixers, the impedance operating to convert the rectified LO voltage into a

common mode even order LO interferer current. The LO interferer can then pass through the mixer core and to the output loads.

[0013] Reduced mixer even-order suppression can be especially problematic when the mixer is integrated with other circuitry. Fig. 2 illustrates one example of such an instance where multiple mixers are supplied by a single VCO. Each mixer is configured to operate in either a mixing mode, whereby the synthesized signal 205 and input signals 210a and 210b are provided to respective mixers 220a and 220b to produce respective mixed signals 230a and 230b, or in a bypass mode, whereby the synthesized signal 205 is not supplied to the mixer 220c and the input signal 210c is routed such that it bypasses the mixer 220c.

[0014] In such a system, the LO even order mixer interferers can couple to the VCO via substrate leakage, indirect conductor leakage (ground, power or logic lines), magnetic or electrostatic coupling, or other such means. Within the VCO, the even order interferers may cause spurs in the VCO output, or may combine with odd order harmonics of the desired signal to produce an interfering signal at the desired frequency of oscillation. In the latter case, the interfering signal will produce a phase offset in the VCO-generated output. If that coupling should change, a phase step will be introduced into the system which the PLL will attempt to correct for. If the phase step is large enough, the consequence can be a disruption of the digital demodulation process.

[0015] What is therefore needed is a new mixer circuit operable in either a bypass mode or mixing mode, and which can maintain a substantially constant level of LO even order interference independent of its operation in either the bypass or mixing mode.

Summary

[0016] The invention described herein provides for a mixer circuit which is operable in either a bypass mode or mixing mode and which can maintain a substantially constant level of LO even order interference while operating within or switching between the bypass or mixing modes. A substantially constant level of LO even order interference can be maintained by: (i) maintaining the circuit path between the IF load and mixer core during both the bypass and mixer modes of operation, and (ii) maintaining mixer operation during bypass mode operation.

[0017] The invention is now summarized in various embodiments, the first of which describes a mixer circuit having a mixer core and a mode select circuit. The mixer core includes first and second switches, each of which has an input switchable between first and second outputs. The mode select circuit is coupled to the mixer core and includes third and fourth switches, which are collectively configured to operate in either a first state corresponding to the bypass mode, or a second state corresponding to the mixing mode.

[0018] The third switch has an input coupled to the second output of the first switch, the input switchable between a first output which is coupled to the first output of the first switch, and a second output which is coupled to the second output of the second switch. The fourth switch has an input coupled to the first output of the second switch, and is switchable between a first output which is coupled to the first output of the first switch, and a second output coupled to the second output of the second switch.

[0019] The input of the first switch is configured to receive a signal at a first frequency, wherein the first and second switches are configured to switch between their respective first and second outputs at a second frequency, and wherein, responsive to the selected output of the third and fourth switches, the first output of the first switch, and the second output of the second switch are each configured to output a signal which is either (i) at the first frequency, or (ii) a mixing product of the first and second frequencies.

[0020] Other embodiments of the invention, as well as particular features of the embodiments will be more readily understood in view of the following drawings and detailed description.

Brief Description of the Drawings

[0021] Fig. 1A illustrates a simplified switch diagram of a doubly balanced mixer as known in the art.

[0022] Fig. 1B illustrates the doubly balanced mixer of Fig. 1A as a Gilbert cell mixer circuit.

[0023] Fig. 2 illustrates a common oscillator, multiple mixer system in which the mixer circuit could be employed.

[0024] Fig. 3A illustrates a simplified switch diagram of a mixer circuit in accordance with one embodiment of the present invention.

[0025] Fig. 3B illustrates a method of operating the mixer circuit shown in Fig. 3A in accordance with the present invention.

[0026] Fig. 3C illustrates the mixer circuit of Fig. 3A as a modified Gilbert cell mixer circuit in accordance with the present invention.

[0027] Fig. 4 illustrates a second embodiment of the mixer circuit in accordance with the present invention.

[0028] Figs. 5A and 5B illustrates common oscillator, multiple mixer systems utilizing the mixer circuits of Figs. 3A and 4 in accordance with embodiments of the present invention.

Detailed Description

[0029] Fig. 3A illustrates a simplified switch diagram of a mixer circuit 300 in accordance with one embodiment of the present invention. The mixer circuit 300 includes a mixer core 320 and a mode select circuit 340. The mixer core 320 includes two input switches 324 and 328, each switch having an input 324a, 328a, and two outputs 324b, 324c, and 328b, 328c, respectively. Switches are depicted to convey the component's general function, and those skilled in the art will readily appreciate that each may be realized using an variety of circuit elements, including transistors (BJT and FET types), diodes, and the like. Accordingly, as used herein, the term "switch" or "switches" shall denote any of these circuit elements, or equivalents thereof.

[0030] Input switches 324 and 328 are operable to accept a signal at a first frequency f_1 in either a differential or single-sided form. In a differential form, the first frequency signal f_1 will consist of a differential signal, wherein separate polarities of the first frequency signal f_1 are supplied to separate switch inputs 110a and 110b, respectively. During single-sided operation, only one of the switches' inputs (e.g., 110a) is needed to receive the first frequency signal f_1. In this embodiment, the input of the other switch (e.g., 110b) is coupled to an ac ground.

[0031] The first and second switches 324 and 328 are further configured to receive a switching signal 125, which operates to switch the first and second switches between their respective output states at a second frequency f_2, as will be further described below. In a particular embodiment shown, the first and second switches 324 and 328 are

configured such that both, upon receiving the switching signal 125, switch to the opposite states (i.e., one to its first output, and the other to its second output). In such an embodiment, the switching signal 125 may be supplied in anti-phase to configure the first and second switches in opposite output states.

[0032] The mixer circuit 300 further includes a mode select circuit 340, implemented in one embodiment as third and fourth switches 344 and 348. Third switch 340 includes an input 344a switchable to two outputs 344b and 344c, and fourth switch 348 includes an input 348a switchable to two outputs 348b and 348c. As shown, the third switch's input 344a is coupled to the second output 324c of the first switch. The third switch's first output 344b is coupled to the first switch's first output 324b, and the third switch's second output 344c is coupled to the second switch's second output 328c. The fourth switch's input 348a is coupled to the second switch's first output 328b. The fourth switch's first output 348b is coupled to the first switch's first output 324b, and a second output 348c coupled to the second switch's second output 328c.

[0033] The third and fourth switches are further configured to receive a mode select signal 350 operable to select the output state of the third and fourth switches 344 and 348. In a specific embodiment, the third and fourth switches 344 and 348 are collectively configured to operate in one of two states: a bypass state or a mixing state. The bypass state is exemplified in Fig. 3A with the third switch 344 coupled to its first output 344b and the fourth switch 348 coupled to its second output 348c as shown in Fig. 3A. The mixing state could be alternatively realized by switching both states of the third and fourth switches, as will be further illustrated below. The resulting bypass or mixed signal is provided in differential form at output ports 130a and 130b. IF loads 365a and 365b are each coupled to a respective output port and an ac ground, as described below. In an alternative embodiment, a single IF load may be coupled between ports 365a and 365b. The term "IF" load shall not infer that the loads' frequency of operation is limited to those frequencies below the input signals, and in fact may be a higher operational frequency when the desired mixing product is an upconverted signal. Further, the IF load may comprise active or passive components as known in the art.

[0034] The switches (or their corresponding implementation in transistors, diodes, or other components) may be discretely or integrally formed using a variety of fabrication

techniques known in the art, including monolithic fabrication in a Bipolar Complementary Metal Oxide Semiconductor (Bi-CMOS) process. Additional circuitry described herein, such as IF loads and oscillator circuitry, as well as other components may be monolithically formed onto an integrated circuit device in accordance with the present invention.

[0035] Fig. 3B illustrates a method for operating the mixer circuit shown in Fig. 3A in accordance with the present invention. Initially at 372, a first frequency signal is supplied to one or both of the input switches 324 and 328. As explained above, the first frequency signal may be in the form of a single-sided signal, in which case the first frequency signal is applied to one of the inputs 110a or 110b, the other switch input being coupled to an ac ground. In the case of an applied differential signal, oppositely polarized signals are supplied to respective signal inputs 110a and 110b.

[0036] Next at 374, the input terminal of the first and second switches is switched between each switch's first and second output at a second frequency f_2. In a specific embodiment, this process is performed by using the second frequency signal as a switch control signal. In such an embodiment, an oscillator or other frequency source used to generate the second frequency signal may be local/integrated with one or more of the switches, or may be externally located and supplied to the first and second switches via a transmission medium.

[0037] Next at 376, the first and second outputs of each input switch are coupled to either: (i) a node common to the switch's first and second outputs, or (ii) nodes of opposite polarity. Connecting the two outputs to a common node results in the first frequency signal being output at 130 (bypass mode), and connecting the two outputs to opposite polarity nodes results in a mixing operation of the first and second frequency signals, and accordingly the generation of one or more mixing products therefrom. The process of 376 is performed by the mode select circuit 340 illustrated in Fig. 3A, whereby in the bypass mode of operation the third switch is configured to connect the first and second outputs of the first switch 324 to a common node 130a, and the fourth switch 348 is configured to connect the first and second outputs of the second switch 328 to a common node 130b. To operate in the alternate mixing mode, the process is performed by switching the states of the third and fourth switches. In this state, the first and second outputs of the first switch 324 will alternately connect to opposite polarity nodes 130a and 130b, and the first and second outputs of the second switch

328 will also alternately connect to opposite polarity nodes 130b and 130a. In this manner, the output states of the third and fourth switches 344 and 348 are configurable either in a bypass mode where the outputs of the first and second switches are connected to a common node, or in a mixing mode where the outputs of the first and second switches are connected to opposite polarity nodes. Further preferably, the connection between the mixer core (first and second switches) and the IF loads 365a and 365b is maintained during operation in either the bypass mode or mixing mode. Additionally, the first and second switches are controlled to continuously switch between their respective outputs at the second frequency during operation in either the bypass or mixing modes. As noted above, a single IF load may be coupled between nodes 130a and 130b in an alternative embodiment under the present invention.

[0038] Fig. 3C illustrates the mixer circuit of Fig. 3A as a modified Gilbert cell mixer circuit 380 in accordance with the present invention, with previously identified components retaining their reference numerals. As depicted, each of the switches 324, 328, 344, and 348 are implemented as a differential pair of npn bipolar junction transistors Q1-Q8. A mixer/bypass control circuit produces a control signal 350 which is supplied differentially to the base terminals of the mode select switches 344 and 348. The polarity of control signal may be reversed to switch circuit operation between bypass and mixing modes. A signal source (e.g., a LO source) is operable to provide the second frequency signal 125 to the mixer core switches 324 and 328. The input signal f_1 is applied to the input terminals 110a and 110b of buffer transistors 117, or alternatively may be provided as a single-ended signal, in which case one of the input terminals 110a or 110b is coupled to an ac ground, as described above.

[0039] In a specific embodiment of the mixer circuit 380, transistors Q1-Q8 are npn bipolar transistors 20 um x 0.4 um, IF loads 365a and 365b are 200 ohms, resistor 115 is 200 ohms, the first frequency signal f_1 operates at 950 - 2150 MHz, the second frequency signal f_2 operates at 3100 MHz, and the mode select signal 350 is 500 mV DC. The circuit's supply V_{cc} operates at +6 VDC. Further specifically, the illustrated components are integrally formed using a 0.35 um Bi-CMOS photolithographic process. Skilled practitioners will appreciate that that the circuit 380 can be alternatively realized using various

modifications, e.g., pnp-type bipolar transistors, n or p-type field effect transistors, or other components such as diodes, and the like.

[0040] Fig. 4 illustrates a second embodiment of the mixer circuit in accordance with the present invention. The mixer circuit 400 includes a mode select switch 410 having an input 410a to receive the first frequency signal f_1, a first output 410b coupled to a bypass circuit 420, and a second output 410c coupled to a mixing core 430. The bypass circuit 420 may be any transmission medium operable to support the propagation of the first frequency signal therealong, including printed/integrated circuit traces (including ungrounded lines or grounded lines such as microstrip, stripline, coplanar waveguide and the like), wire, twisted pair line, coaxial cable, conductive or dielectric waveguide, and the like. The mixer core 430 has an input coupled to the switch's second output 410c, a second input operable to receive the second frequency signal 125, and an output. The mixer core 430 can be of any conventional type (i.e., single-ended, singly-balanced, doubly balanced, etc.) and realized in any of the known forms, such as a Gilbert cell mixer.

[0041] The mixer circuit further comprises a signal combiner 440 coupled to the bypass circuit 420 and the mixer output. The signal combiner 440 has an output coupled to a common load 450. The signal combiner may be realized as a commonly connected port, power combiner (active or passive), or similar circuits. Selection of the bypass or mixing mode is provided by a mode select signal 350, which is supplied by a control circuit. The mixer core 430 is supplied the second frequency signal 125 via a local oscillator. One or more of the described components may be integrally fabricated into a monolithic circuit using semiconductor processing techniques appropriate for the particular material. Preferably, the operation of the mixer core continues and circuit connections between the mixer core 430 and the common load 450 is maintained during operation within or switching between the bypass and mixing modes.

[0042] Figs. 5A and 5B illustrate exemplary systems using the improved mixer circuit of Fig. 3A or 4 in accordance with the present invention, the exemplary systems comprising a common oscillator, multiple mixer system. Referring first to Fig 5A, the system 520 includes a frequency synthesizer 522 and a VCO 524 coupled to three mixer circuits $380_{1\text{-}3}$, the detailed architecture of each being described in Figs. 3A and 3C, above. The frequency synthesizer 522 and VCO 524 operate to produce the second signal frequency

f_2, which is supplied to each of the three mixer circuits 380_{1-3}. Each mixer circuit 380_{1-3} is additionally supplied with a first frequency signal 312_{1-3} in differential form. Each first frequency signal 312_{1-3} is identified as f_1 for convenience, and the reader will appreciate that each of these frequencies may be different.

[0043] The mixer circuits 380_{1-3} are supplied respective mode select signals 350_{1-3} to configure each corresponding mixer circuit to their desired output. In the shown embodiment, the first mixer circuit 380_1 is supplied a "bypass" mode signal 350_1, resulting in the (differential) output at the first signal frequency f_1. The second mixer circuit 380_2 is supplied a "mix" mode signal 350_2, resulting in the output of the mixing product described above. Similarly, the third mixer circuit 380_3 receives the first and second frequency signals f_1, f_2, and the "mix" mode signal 350_3, resulting in the mixing mode of operation. Preferably, the first and second switches of each mixer circuit 380_{1-3} continues to switch at the second frequency f_2 regardless of whether the supplied control signal 350_{1-3} sets the mixer circuit to a bypass mode or mixing mode. Additionally, the mixer circuit's coupling to the IF loads 365a and 365b (or to a single IF load coupled between differential nodes 130a and 130b) is maintained during and switching between the bypass and mixing modes.

[0044] Fig. 5B illustrates another embodiment of a common oscillator, multiple mixer system 550 in which the mixer circuit of Fig. 4 is employed. The system 550 similarly employs a frequency synthesizer 522 and a VCO 524 for generating the second frequency signal f_2 which is commonly supplied to the mixer circuits 400_{1-3}. In this system, the first frequency signal 312_{1-3} (identified as f_1 for convenience only) is supplied to the input of each mixer circuit. A corresponding mode select signal 350_{1-3} is also supplied to set the switches in the desired bypass or mixing mode enabling the independent control of each mixer circuit in either a bypass or mixing mode. As described above with respect to the mixer embodiment of Fig. 4, the operation of the mixer continues and circuit connections between the mixer core 430 and the common load 450 can be maintained during operation within or switching between the bypass and mixing modes in order to maintain a substantially constant level of LO even-order interference.

[0045] When operated in the aforementioned manner, the mixer circuits of the present invention retain a substantially constant level of LO even-order interference whether they are operating within, or are switched between a bypass or mixing mode state.

Consequently, the mixers' even order interferers will (i) produce substantially constant spurious products in the VCO output which typically fall outside of the PLL loop bandwidth, and/or (ii) combine with odd order LO products to produce a substantially constant phase-offset at the desired VCO frequency, which can be easily corrected by the PLL.

[0046] While the above is a detail description of the present invention, it is only exemplary and various modifications, alterations and equivalents may be employed in various apparati and processes described herein. Accordingly, the scope of the present invention is hereby defined by the metes and bounds of the following claims: